A look into the CXL device ecosystem and the evolution of CXL use cases
CXL Board of Directors

Industry Open Standard for High Speed Communications

240+ Member Companies

Compute Express Link™ and CXL™ are trademarks of the Compute Express Link Consortium.
Industry focal point

CXL is emerging as the industry focal point for coherent IO

- CXL Consortium and OpenCAPI sign letter of intent to transfer OpenCAPI specification and assets to the CXL Consortium

- In February 2022, CXL Consortium and Gen-Z Consortium signed agreement to transfer Gen-Z specification and assets to CXL
Industry Liaisons

CXL is collaborating with industry organizations.
CXL Delivers the Right Features & Architecture

Challenges

- Industry trends driving demand for faster data processing and next-gen data center performance
- Increasing demand for heterogeneous computing and server disaggregation
- Need for increased memory capacity and bandwidth
- Lack of open industry standard to address next-gen interconnect challenges

CXL
An open industry-supported cache-coherent interconnect for processors, memory expansion and accelerators

Coherent Interface
Leverages PCIe™ with 3 mix-and-match protocols

Low Latency
Cache and Memory targeted at near CPU cache coherent latency

Asymmetric Complexity
Eases burdens of cache coherent interface designs

www.ComputeExpressLink.org
Data Center: Expanding Scope of CXL

CXL 1.1
- Single Node Coherent interconnect
- Multiple Nodes inside a Rack/Chassis supporting pooling of resources

CXL 2.0
- Compute Express Link™ and CXL™ are trademarks of the Compute Express Link Consortium.
- Memory/Accelerator Pooling with Single Logical Devices
- Multiple Nodes inside a Rack/Chassis supporting pooling of resources

CXL 3.0
- Composable Fabric growth for disaggregation/pooling/accelerator
- Memory Pooling with Multiple Logical Devices

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## CXL Spec Feature Summary

<table>
<thead>
<tr>
<th>Features</th>
<th>CXL 1.0 / 1.1</th>
<th>CXL 2.0</th>
<th>CXL 3.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Release date</td>
<td>2019</td>
<td>2020</td>
<td>August 2022</td>
</tr>
<tr>
<td>Max link rate</td>
<td>32GTs</td>
<td>32GTs</td>
<td>64GTs</td>
</tr>
<tr>
<td>Flit 68 byte (up to 32 GTs)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Flit 256 byte (up to 64 GTs)</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Type 1, Type 2 and Type 3 Devices</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Memory Pooling w/ MLDs</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Global Persistent Flush</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CXL Integrity and Data Encryption (IDE)</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Switching (Single-level)</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Switching (Multi-level)</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Direct memory access for peer-to-peer</td>
<td></td>
<td></td>
<td>✓</td>
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<tr>
<td>Enhanced coherency (256 byte flit)</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Memory sharing (256 byte flit)</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Multiple Type 1/Type 2 devices per root port</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Fabric capabilities (256 byte flit)</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>
CXL Ecosystem & Demos and Evolving Use Cases
CXL Ecosystem

Growth of CXL Ecosystem since its inception

- Ecosystem that meets the ever-increasing performance and scale requirements
- Fully backwards compatible
- Lowers overall system cost
- Comprehensive compliance and testing support
Evolving Use Cases

**CXL Memory Expansion**
- Improves processor efficiency
- Increases Capacity
- Improves Bandwidth
- Lowers TCO

**CXL-Enabled Tiered Expansion**
- Flexible support for faster-slower Memory Tier
- Lowers TCO - higher memory capacity for cheaper $/GB
- Improves Bandwidth

**Pooled Memory**
- Reduces Memory Stranding
- Improves Data Flow Efficiency
- Improves Memory Utilization
- Lowers TCO

**Shared Memory**
- Scales to large datasets
- Flexibility across the fabric
- Improves Memory Utilization
- Lowers TCO

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Memory Pooling allows a host or multiple hosts to expand their memory capacity and bandwidth by using unique areas in a memory device with allocation of Memory segments tied to a unique host established at boot or a hot-swap event (i.e. memory segments accessed by a single host at runtime but can be migrated from host to host as needed).

Memory Sharing allows multiple hosts to coherently share a common memory area in one or multiple memory devices. Multiple hosts can concurrently access and operate on that shared memory.
CXL Demos at SC’22

CXL Memory Solutions

- AMD SEV Enabled Confidential Containers on CXL Encrypted Memory
- CXL from Promise to Reality with Real Silicon on Customer Platforms
- Rack-Scale Memory Pooling with CXL
- CXL-based SMC 2000 Smart Memory Controllers
- CXL Memory Expansion with Intel Archer City PDK
- AL/ML Application on CXL Memory Expander with Scalable Memory Development Kit (SMDK)
- CXL-based Smart Memory Node™
CXL Demos at SC'22

**CXL IP. Compliance and Testing**
- **Intel**: CXL™ Type 2 Compliance & Traffic Demo using 4th Gen Intel Xeon Scalable Processors and Intel FPGAs
- **Synopsys**: Synopsys CXL 2.0 IP Successful Interoperability and Compliance Testing

**CXL Fabric and Switch Solutions**
- **IntelliProp**: Disaggregated and Composable CXL attached Memory Fabric
- **XConnTech**: CXL Memory Pooling with a CXL Switch

**CXL Software Solutions**
- **MemVerge**: Software for Memory Visualization, Tiering & Pooling

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CXL at SC’22

• CXL is gaining momentum!
  • SC’21: 5 live CXL demos
  • SC’22: 12 live CXL demos

• CXL was recognized in the annual HPCWire Editors’ Choice Award for Best HPC Interconnect Product or Technology

• View CXL technology demos: www.ComputeExpressLink.org/sc-22
Q&A Panel
CXL Demos at SC’22

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Thank You

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